Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-7. (canceled)

8. (currently amended) ~~The apparatus of claim 6,~~ An apparatus for writing a target address of a taken branch instruction into a branch target address cache (BTAC) upon execution of the taken branch instruction, the BTAC having a plurality of storage elements for caching target addresses of executed branch instructions, each of the plurality of storage elements comprising first and second entries for storing a target address, the apparatus comprising:

a global indicator, for specifying a global one of the first and second entries of the BTAC plurality of storage elements; and

branch control logic, coupled to said global indicator, for selecting one of the first and second entries to write the taken branch instruction target address into based on said global indicator, wherein said global one of the first and second entries specifies which of the first and second entries was last written to in any one of the plurality of storage elements when both of the first and second entries therein were invalid, wherein said branch control logic selects an opposite of said global one of the first and second entries specified in said global indicator to write the taken branch instruction target address into, wherein said branch control logic updates said global indicator to specify said selected entry, wherein the plurality of storage elements also includes a valid indicator associated with each of the first and second entries, for indicating whether the target address stored therein is valid or invalid, wherein if only one of the first and second entries is invalid in one of the plurality of storage elements that is selected for updating, said branch control logic selects said invalid entry to write without regard to said global indicator.

9. (canceled)

10. (currently amended) ~~The apparatus of claim 9,~~ An apparatus for writing a target address of a taken branch instruction into a branch target address cache (BTAC) upon execution of the taken branch instruction, the BTAC having a plurality of storage elements for caching target addresses of executed branch instructions, each of the plurality of storage elements comprising first and second entries for storing a target address, the apparatus comprising:

a global indicator, for specifying a global one of the first and second entries of the BTAC plurality of storage elements; and

branch control logic, coupled to said global indicator, for selecting one of the first and second entries to write the taken branch instruction target address into based on said global indicator, wherein said global one of the first and second entries specifies which of the first and second entries was last written to in any one of the plurality of storage elements when both of the first and second entries therein were invalid, wherein said branch control logic selects an opposite of said global one of the first and second entries specified in said global indicator to write the taken branch instruction target address into, wherein said branch control logic updates said global indicator to specify said selected entry, wherein the plurality of storage elements also includes a valid indicator associated with each of the first and second entries, for indicating whether the target address stored therein is valid or invalid, wherein the BTAC comprises a least recently used indicator associated with each of the plurality of storage elements for indicating which of the first and second entries in said associated storage element was least recently used, wherein if both of the first and second entries are valid in one of the plurality of storage elements that is selected for updating, said branch control logic selects one of said valid first and second entries to write based on said least recently used indicator without regard to said global indicator.

11-32. (canceled)